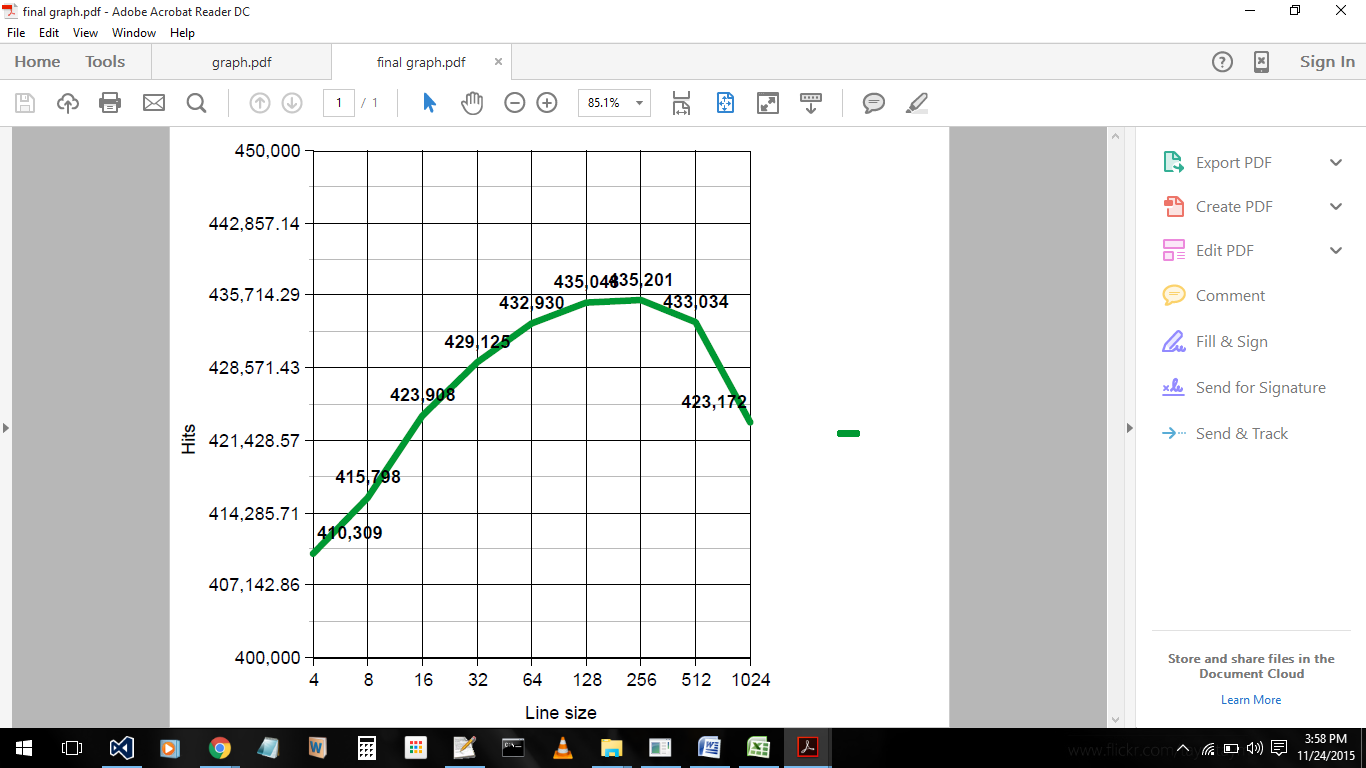
**CMPS-5133 Advanced Computer Architecture**

Cache Simulation Project.

By

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 In this project, we have simulated the 5-way set associative cache simulation in C++. The total size of the cache is 10240 Byes. The simulation works for different line sizes like 4, 8, 16, 32, 64, 128, 256, 512 and 1024. The total number of hits and misses is calculated for each line size. Number of hits with line size is graphed, as shown in the figure below.

|  |  |  |
| --- | --- | --- |
| **Line Size** | **Number of hits** | **Number of misses** |
| 4 | 310309 | 36392 |
| 8 | 415798 | 30903 |
| 16 | 423908 | 22793 |
| 32 | 429125 | 17576 |
| 64 | 432930 | 13771 |
| 128 | 435048 | 11653 |
| 256 | 435201 | 11500 |
| 512 | 433034 | 13667 |
| 1024 | 423172 | 11500 |

**Conclusion:**

As shown in the graph the total number of Hits is more for the line size of 256 Bytes. By this, we propose that when a 5 - way set associative cache with cache size of 10240 Bytes is designed, 256 Bytes of line Size is recommended to get minimum number of misses or maximum number of hits. The number of hits and misses is also tabulated.